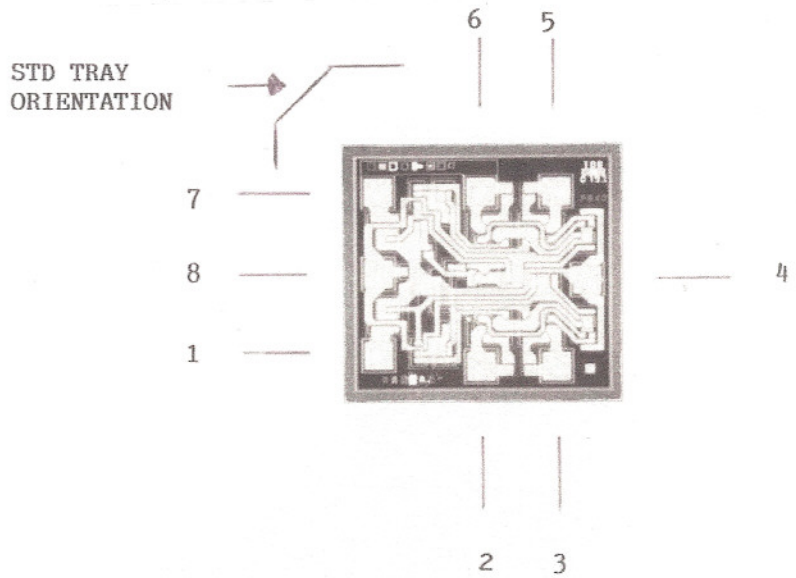
Sierra Components, Inc.

2222 Park Place • Suite 3E • Minden, Nevada 89423
Phone: 775.783.4940 Fax: 775.783.4947

Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



Pin Function
1. **OUT (1)**
2. **IN- (1)**
3. **IN+ (1)**
4. **Vcc-**
5. **IN+ (2)**
6. **IN- (2)**
7. **OUT (2)**
8. **Vcc+**

Backside bias = Vcc-
Standard Tray: H20-055-24

Mask Ref:P840

APPROVED BY:	**DG**	**DIE SIZE :1.08 x 1.08mm**	**DATE: 1/24/07**
MFG: CFS Thompson		**THICKNESS:**	**P/N:LM193/393**